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FURTHER IMPROVEMENTS TO A DIFAR MULTIPLEXER- DEMULTIPLEXER SYSTEM

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UNDERWATER SYSTEMS DEPARTMENT

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This report describes the updated version of a multiplexer-demultiplexer system for DIFAR signals designed by U20, Sensors & Electronics Division. Theory, circuitry and performance are provided.

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FOREWORD

This report describes the updated version of a multiplexer-demultiplexer system for DIFAR signals designed by U20, Sensors & Electronics Division. Theory, circuitry and performance are provided.

Approved by:

C. A. KALIVRETENOS, Head
Sensors and Electronics Division

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BACKGROUND

Over the years, many DIFAR system multiplexers and demultiplexers have been designed and built at NSWC-WO. Numerous changes have been made since the system was last described in a classified report. Inasmuch as the basic DIFAR system was declassified (OPNAVINST 5513.2B encl. 82) after the last report was issued, this seemed like an appropriate time to document the latest system modifications in an unclassified format. A complete description is included here, obviating the need for the previous classified report.

INTRODUCTION

A DIFAR Sonobuoy has an omnidirectional hydrophone (OMNI), a dipole effectively oriented along a (magnetic) North-South axis (N-S), and a dipole effectively oriented along an East-West axis (E-W). Before transmission over the RF link the three signals are multiplexed as shown in Figure 1. The OMNI occupies baseband. The two dipoles are modulated by quadrature phases of a 15 KHz subcarrier. A 15 KHz pilot tone is added as phase reference necessary for the demultiplexer. A 7.5 KHz signal derived from the 15 KHz is added as frequency reference to assist the demultiplexer in finding the 15 KHz signal. The 15 KHz subcarrier may have sideband information close by which could be mistaken for the reference. The 7.5 KHz occupies a vacant portion of the spectrum and hence prevents this ambiguity. The function of the demultiplexer is to convert this spectrum back to three channels of baseband information. It does this by generating a local subcarrier locked to the received subcarrier, and using this local subcarrier to demodulate the dipole signals back to baseband. The OMNI is recovered simply by low-pass filtering.

MULTIPLEXER OPERATION

A block diagram of the multiplexer is shown in Figure 2. The input signals are band-limited by low-pass filters to prevent frequency aliasing or noise around the 7.5 KHz pilot, should high frequency components be present in the input signals. The dipole signals are modulated up in frequency by quadrature phases of 15 KHz. They are then summed together with the OMNI and the two pilot tones to form the composite signal. The composite signal is low-pass filtered, as square waves are used for the subcarriers and modulators, causing unwanted harmonic frequency components.

DEMULTIPLEXER OPERATION

A block diagram of the demultiplexer is shown in Figure 3. The OMNI signal is recovered by low-pass filtering. The dipole signals are translated to baseband by multiplying by quadrature phases of 15 KHz and low-pass filtering.

The 15 KHz is obtained by tracking the 15 KHz pilot tone with a phase-lock loop (PLL). The PLL acts as a very narrow tracking filter, tracking the pilot in frequency and phase but filtering out the sideband information.

The PLL used is actually a double loop. A 15 KHz loop performs the function just described. A 7.5 KHz loop locks on to the 7.5 KHz signal, and performs the functions of acquisition and frequency reference. It cannot provide the phase reference by itself, as the relative "phase" between the 15 KHz and 7.5 KHz signals cannot be guaranteed. The 15 KHz signal applies the necessary phase correction to the 7.5 KHz loop.

The 7.5 KHz is first isolated by a narrowband filter and then clipped. The detector in the 7.5 KHz loop is a digital frequency-phase comparator circuit (Reference 1) triggered on the edges of the input signal and the reference (VCO), respectively. The average output of the circuit is linearly proportional to phase difference of the inputs over the full $\pm 360°$ range (see Figure 4a). This corresponds to $\pm 720°$ at 15 KHz, so any possible phase correction may be applied by the 15 KHz loop without exceeding the linear range of 7.5 KHz detector. The output of the phase-frequency comparator is applied to the 7.5 KHz integrator, which slews the VCO (voltage-controlled oscillator) until the reference is the same frequency as the input and in phase. The direct path around the integrator is necessary to provide loop damping.

Note that the 7.5 KHz loop is self-acquiring, since if more transitions occur at one input than the other, the circuit remains in the corresponding state, slewing the integrator in the proper direction. Note also that with this detector, proper polarity must be observed. Overall feedback can be either negative, in which case the loop will acquire and track; or positive, in which case the loop will instead avoid the signal.

When the 7.5 KHz loop is locked in frequency, the 15 KHz loop by definition is also locked in frequency, but not necessarily in phase. An error voltage is developed at the output of the multiplier proportional to the cosine of phase difference (Figure 4b). This slews the 15 KHz integrator, which applies a bias to the 7.5 KHz integrator. The 7.5 KHz loop must then track at some phase difference other than 0° to offset the bias. Polarity in the 15 KHz part of the loop is irrelevant, as with the multiplier detector either slope is available. If loop gain happens to be positive the VCO merely increases phase error until the stable slope is reached.

The system reaches equilibrium when the VCO matches both inputs in frequency, the 15 KHz reference is in quadrature with the 15 KHz input, and the 7.5 KHz reference is somewhere in the range -90° to +90° with respect to the 7.5 KHz input, depending on the relative "phase" between the incoming 15 KHz and 7.5 KHz.

If the 7.5 KHz loop is made much faster than the 15 KHz loop, operation of the two loops is essentially independent. The system tracks the 7.5 KHz but adjusts the phase by the 15 KHz. The requirements are that: (1) the inner loop

[1] Reed. L. W., and Treadway, R. J., "Test Your PLL IQ," EDN Magazine, 20 Dec 1974.

be able to keep up with absolute frequency-phase changes of the 7.5 KHz signal; (2) the outer loop be able to keep up with relative "phase" changes between the 15 KHz and the 7.5 KHz signals; and (3) the latter occur much more slowly than the former. These requirement are all easy to satisfy.

CHANGES

The changes from the previous multiplexer design are, briefly: Gain adjustment on each of the three inputs is now done by pots instead of trimming resistors. Channel bandwidth has been increased from 2.5 KHz to 5 KHz by using more sophisticated filters. The filters are also configured to have notches at 7.5 KHz and 15 KHz, better eliminating interference between the signals and the subcarriers. The crystal oscillator has been changed. A balance adjustment has been added to the modulators; some were good enough without it and some were not, depending on the manufacturer. The biasing and gains in the summation network have been changed. The standard (which has changed several times) at this moment is that the power in the dipoles (together) shall equal that in the OMNI, and the subcarriers shall have an amplitude of 100 mVRMS (each). An overall gain adjustment has been added to the output, so there are four gain adjustments for the five components of the output. Basically what cannot be adjusted is the amplitude of the 7.5 KHz subcarrier, but this is not at all critical anyway. The phase of the dipoles relative to the OMNI has been inverted by rearranging the transistor current source after the modulators. The original multiplexer was made to agree with an AQA-7 which was later found to have been wired backwards. The new arrangement also eliminates two precision resistors.

In the demultiplexer, the 7.5 KHz filter has been changed. It is sharper now, but does require adjustment. It now uses the same precision capacitors as the filters. It has been biased differently for better dynamic range. The VCO now uses a variable capacitor instead of a variable inductor. The latter picked up hum from the power supply transformer, requiring shielding, and was also sole-sourced. The bias on the lock indicator has been changed to make it require less carrier amplitude.

MULTIPLEXER CIRCUITRY

Multiplexer circuitry is shown in Figure 5. The input filters are identical 5-pole low-pass filters having a cutoff frequency of 5 KHz. Each filter consists of a ladder of series resistors and shunt active "D" elements (also called super-capacitors or frequency-dependent-negative-resistors) (Reference 2), terminated at each end with an inductor and capacitor. The inductor improves the filter characteristic by improving the usual capacitive termination (Reference 3). Zeroes have been added at 7.5 KHz and 15 KHz by adding resistors in series with the super-capacitors. The filter characteristic is shown in Figure 6.

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[2] Burton and Treleven, "Active Filter Design Using Generalized Impedance Converters," EDN Magazine, 5 Feb 1973.

[3] Delagrange, A. D., "A Useful Filter Family," NSWC/WOL TR 75-170, 20 Oct 1975.

High-speed balanced modulators are used for the multipliers so negligible phase shift is contributed. The balance adjustments previously eliminated have been reinstated. Offset here causes carrier feedthrough. On the E-W channel this does not matter much, but on the N-S channel it causes phase error in the 15 KHz pilot.

The 15 KHz is derived from a 60 KHz crystal oscillator by a divide-by-four shift register counter. The 7.5 KHz is generated from the 15 KHz by a divide-by-two-counter. The CMOS logic clamps nicely to the power supply, giving a standardized voltage.

The five signals are summed by a resistor network and low-passed by a 5-pole passive L-C ladder filter having a cutoff frequency of 24 KHz. The ladder is terminated at both ends by resistances, the summing network being the input termination. This arrangement prevents exceeding the slew rate of the output op-amp, which could cause asymmetrical distortion of the signal and hence unwanted phase shifts. The output filter characteristic is shown in Figure 7. Across the information bands, particularly the dipole bands, amplitude must be constant and phase shift linear. Otherwise the sidebands are altered and the independence of the dipoles is lost.

DEMULTIPLEXER CIRCUITRY

The multiplier in the 15 KHz PLL (Figure 8) is actually the N-S balanced modulator of the demultiplexer. For the proper combination of input frequencies and output filtering a balanced modulator acts as a linear multiplier; that is the case here. The output must be taken differentially, as the common-mode voltage of the balanced modulator circuit is subject to DC drift, which is not allowable here. The balanced modulator is similar to that used in the multiplexer, but the biasing has been changed to double the dynamic range. This is not necessary in the multiplexer where each modulator handles only one signal, as opposed to all three signals plus two subcarriers in the demultiplexer.

This method has the advantage that the gain in the 15 KHz loop, and hence the loop parameters, do not vary with modulation level or power supply voltage. The disadvantage is that they do vary, however, with input carrier amplitude. The input buffer is unity gain and assumes a 15 KHz carrier level of around 100 mVRMS. The 7.5 KHz carrier level should be roughly equal to the 15 KHz.

The integrator is a differential integrator. A balance adjust zeroes integrator error, as imbalance would cause the loop to track with a phase error to compensate. Adjustments must be redone if the supply is changed. If the input signal is removed for a long time, the integrator will drift off and saturate. It could then reacquire too near the edge of its range. Therefore, a hi-lo threshold detector senses if the integrator exceeds the center 60% of its range. If this occurs, forward bias is momentarily applied to a field-effect transistor which discharges the feedback capacitor, returning the integrator to the center of its range.

The 7.5 KHz filter consists of an op amp with a bridged-tee as the feedback path. Near the resonant frequency the gain of the bridged-tee is low so the overall filter gain is high. A trimming resistor has been added to get maximum

output at 7.5 KHz, as the filter is narrower than the previous design. A comparator clips the 7.5 KHz signal. Hysteresis is necessary to prevent extraneous zero crossings from noise, as the 7.5 KHz detector will not tolerate these. The filter input is taken from in front of the input buffer, as large signal peaks can saturate the buffer, which would cause momentary loss of the 7.5 KHz. The previous filter was found to give insufficient rejection at 15 KHz, so an LC low-pass was added after it; this has been retained.

The 7.5 KHz detector circuit operates thusly: A positive transition on either input sets that particular flip-flop. It stays set until the other flip-flop gets set. An "AND" gate senses this condition and immediately resets both flip-flops. Thus one flip-flop output corresponds to "faster" pulse and the other to a "slower" pulse, and the two are mutually exclusive. If the input frequency is higher than the VCO frequency, a "faster" pulse occurs each time an extra transition occurs at the input, slewing the integrator to raise the VCO frequency. No pulses occur at the "slower" output (except for a very narrow spike during the reset). The reverse occurs if the VCO frequency is higher. If the frequencies are the same but the input leads the VCO in phase, a "faster" pulse will occur each cycle beginning at the input transition and ending at the VCO transition, reducing the phase lag of the VCO. Again, the reverse happens if the VCO leads. Since the circuit works over a range of $\pm 360°$, the definition of which signal leads does depend on the history of events. This is not relevant in this application, as the loop settles to 0° phase difference.

The output of the new detector circuit is differential, but the flip-flops also have a complement output, so this is used for one and the two then simply added to avoid using another differential integrator. CMOS logic clamps nicely to the power supply and ground, inherently providing pulses of standardized voltage.

The 7.5 KHz integrator has a resistor in series with the feedback capacitor to effect the necessary direct path. This resistor is bypassed with a capacitance chosen to block the AC signals while not affecting the loop response significantly. (The 15 KHz integrator does not require this resistor because the 7.5 KHz loop is so much faster that it provides the damping.) The 7.5 KHz integrator need not be balanced precisely, as the 15 KHz loop adjusts the phase anyway.

The VCO is an LC oscillator to minimize jitter and drift. An op amp provides the necessary gain; a DC bias path insures that the op amp cannot stay in a saturated state. The capacitance is controlled by varying the voltage across a back-biased diode. The oscillator runs at 60 KHz. A divide-by-four shift-register counter gives quadrature phases of 15 KHz. A divide-by-two triggered from an arbitrary phase of the 15 KHz gives the 7.5 KHz.

A second balanced modulator driven in quadrature from the first detects the 15 KHz carrier when the loop is locked on. An averager and comparator give a lock indication when the rectified and averaged signal exceeds a preset threshold. Note that this indicates basically that the loop is locked in frequency; it may or may not have settled to the necessary phase accuracy yet.

A second comparator gives an overload indication if the output of the balanced modulator exceeds a second threshold, indicating too much modulation on

the carrier. The indicator cannot be precise as overload may occur first on either balanced modulator, depending on which dipole has the larger signal. The indicator is therefore set to come on somewhat before overload actually occurs.

The output filters (Figure 9) are the same as the ones used at the multiplexer inputs. The dipole signals are taken from the two balanced modulators; the OMNI comes directly from the input buffer. The inductor has an additional advantage here in that it prevents the slow filter op-amps from being driven into nonlinear operation by the high frequency components of the balanced modulator outputs by slowing the fast-rise steps.

LOOP ANALYSIS

It is necessary to analyze the loop as a feedback system to predict its dynamic behavior. Methods similar to Reference 4 may be used and flow-graphs (Reference 5) are of help. A block diagram and corresponding flow graph of the double loop is shown in Figure 10. All transfer functions are written in terms of phase. Note that the gain of the VCO at the 15 KHz output is thus twice that at the 7.5 KHz output. Note also that the gain of the 15 KHz detector differs from that of the 7.5 KHz detector by a factor c, which depends on subcarrier input amplitude.

Only the poles (roots of the denominator) of the transfer function need to be determined for stability analysis. The flow graph may be simplified by combining parallel branches and ignoring inputs and outputs, as shown in Figure 11a. The poles occur when the loop gain is equal to +1. The polynominal is found to be:

$$S^3 + K_\phi K_V d\, S^2 + K_\phi K_V \left(\frac{1}{\tau_1} + \frac{2cd}{\tau_2}\right) S + 2c\frac{K_\phi K_V}{\tau_1 \tau_2} = 0$$

indicating a third-order system.

The roots of this polynomial can be found, but the expressions are hopelessly involved. Instead, assume that the 15 KHz integrator is enough slower than the 7.5 KHz integrator that at the natural frequencies of the 7.5 KHz loop the gain of the 15 KHz integrator is much less than unity so it does not add a significant contribution. The 7.5 KHz loop alone is shown in Figure 11b. The poles are found to be

$$S = \frac{-K_\phi K_V d \pm \sqrt{(K_\phi K_V d)^2 - 4\frac{K_\phi K_V}{\tau_1}}}{2}$$

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[4]Gardner, Phaselock Techniques, Wiley, 1966.
[5]Mason and Zimmerman, Electronic Circuits, Signals, and Systems, Wiley, 1960.

The 7.5 KHz loop behaves as a normal second order loop. For reasonable values the poles are a complex pair with a natural radian frequency:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{\tau_1}}$$

and a damping ratio:

$$\delta = \frac{d}{2}\sqrt{K_\phi K_V \tau_1} = \frac{d}{2}\omega_n \tau_1$$

(the usual equations).

The poles of the 15 KHz loop are found as follows. The transfer function of the 7.5 KHz loop along the branch common to both loops is found. This function is evaluated for $S \to 0$, since the 7.5 KHz loop is operating far below its natural frequency. The result $(-1/K_\phi)$ is substituted for the upper loop (Figure 11c). The 15 KHz loop is then found to have a single real pole at:

$$S = -\frac{2c}{\tau_2}$$

The 15 KHz loop behaves as a simple first-order system having a time constant:

$$T = \frac{\tau_2}{2c}$$

The speed of 7.5 KHz loop removes the effects of the integrating VCO, so one detector simply adjusts the other and the only factors that matter are the relative gain and the integrator time constant.

DERIVATION OF LOOP PARAMETERS

The circuit parameters are found as follows: The integrator time constant is the product of the input resistor and the feedback capacitor, (1 megohm) times (1 microfarad) = 1 sec for both integrators. The direct path gain added to the 7.5 KHz integrator is the ratio of the feedback resistor to the input resistor, 10 kilohm divided by 1 megohm = .01.

The phase detector characteristic is the average (DC) voltage out of the detector versus the phase difference between the inputs; the phase detector gain is the slope of this curve at the point of loop equilibrium. The 7.5 KHz detector changes linearly from 0V to +15V in 2π radians, so the gain is $15V/2\pi$ = 2.4V/rad everywhere. The 15 KHz phase detector outputs for 0 and $\pi/2$ rad phase difference inputs are shown in Figure 12. It is not immediately obvious that the average value varies sinusoidally, as shown in Figure 4b. To see that the detector characteristic is indeed sinusoidal recall that the balanced modulator multiplies a sine wave by a squarewave, which can be represented as a sine wave plus harmonics. Only the fundamental will contribute to the DC component, so we essentially have the product of sinusoids. This generates only more sinusoids, and the term with nonzero average will be sinusoidal in phase difference. The maximum occurs at 0 rad where the waveform is a full-wave-rectified sine wave (Figure 12a). The average of this waveform of unit amplitude is $2/\pi$, found by integrating the sinusoidal peaks. At $\pi/2$ rad (see Figure 12b) the average is clearly 0; this is where the loop will stabilize. The slope of a unit sine wave at the origin is unity. The peak of a 1 VRMS sine wave is $\sqrt{2}$V. The phase detector output is differential giving a gain of 2. The detector gain is therefore (0.1) $2(2\sqrt{2}/\pi)$ = 0.18 V/rad.

The VCO gain must be found experimentally. The loop is made to track 7 KHz and 8 KHz and the respective 7.5 KHz integrator output voltages noted. The VCO gain is then $2\pi 1000/\Delta V$. The VCO measured was 3430 rad/V. There will be some variation due to the variable capacitors, but it should not be significant.

The parameters of the loop are then:

K_0 = 15V/cycle = 2.4V/rad

K_V = 545 Hz/V = 3430 rad/V/sec

d = .01

τ_1 = 1 sec

τ_2 = 1 sec

c = (0.18V/rad)/(2.4V/rad) = .075 (assuming 0.1 VRMS 15 KHz carrier)

Substituting:

ω_n = 91 rad/sec = 14 Hz

δ = 0.45

T = 6.7 sec

PERFORMANCE

The demultiplexer expects a level of 100 mVRMS (-20dB) for each subcarrier. At about 5 dB below this the lock indicator light goes out, although the demultiplexer is still working. At 10 dB below the desired level the loop is still tracking, but the phase error is serious. Should the levels happen to be higher than expected, performance actually improves, as long as the overload indication is not on. As mentioned, the overload light is set to come on slightly before clipping, so if the light flashes occasionally the system is still working. In fact, the loop will still track if overloaded, but there is phase error due to the nonlinearity from clipping.

Figure 13 shows the performance as noise is added to the demultiplexer input signal. The subcarrier level was kept constant. A 1 VRMS 1 KHz sine wave was put on the OMNI and N-S. Noise of 20 KHz bandwidth was added to the composite signal. Output SNR was taken as the ratio of the signal at the N-S output to the extraneous signal plus noise at the E-W output. Input SNR was taken as the ratio of one subcarrier to the total input noise; it could also be represented as the ratio of the input signal to the noise by adding 20 dB to each of the numbers on the horizontal scale.

Figure 14 gives the allowable amplitude in for a pure tone. The problem is that strong lines at low frequency show up in the composite spectrum next to the 15 KHz subcarrier and fall within the bandwidth of the tracking loop. Since the loop transfer function is single pole-pair, this curve rises at 20 dB/decade. It flattens out at the low end because these frequencies are rejected at 6 dB/octave by the input filtering. It flattens out at the high end because overload occurs. The latter of course depends on how many inputs have signals, as indicated. This applies only to testing, as for real-world signals the signals in the dipole channels uniquely determine the amplitude of the OMNI signal. The curve rises again past 5 KHz because of the input filter cutoff until the filters themselves overload. Note that although the allowable input at low frequencies is quite small, this is not a serious problem because real-world signals are normally broadband.

Figure 15 shows the error between dipole channels, both phase and amplitude, for a multiplexer-demultiplexer pair picked at random. Phase error translates directly to DIFAR bearing error. An amplitude error of 0.3 dB translates to 1° bearing error, worst case. The errors become worst at the band edges, due to mismatch of the filters. Figure 16 similarly shows the errors between one dipole and OMNI. The error here is also influenced by the multiplexer output filter.

POWER REQUIREMENTS

The multiplexer uses $\pm$15 volt supplies at 60 milliamps. The demultiplexer also uses $\pm$15V, at 65 milliamps excluding indicator lights. In either case, $\pm$12V will also work, but the pilot tones will be slightly low for the multiplexer and the demultiplexer will have to be rebalanced. Power supplies should be set within $\pm$ 15 millivolts. If this is not possible, the demultiplexer must be balanced with the power supply it will actually be used with. Adjustment procedures are given in the appendices.

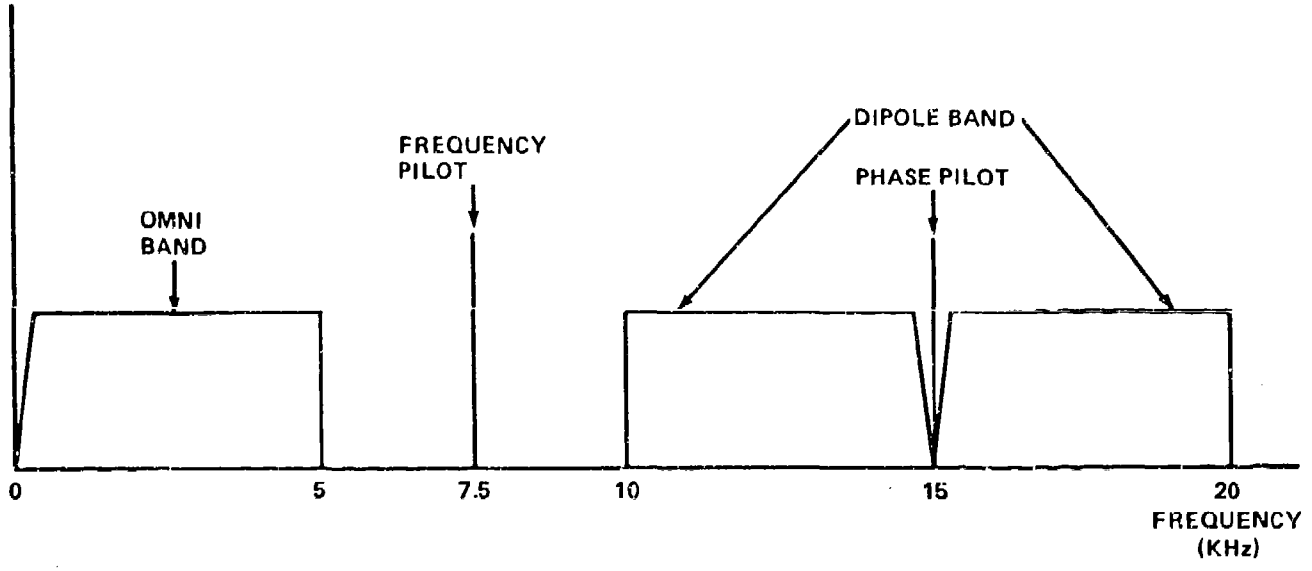


FIGURE 1. SPECTRUM OF MULTIPLEXED SIGNALS

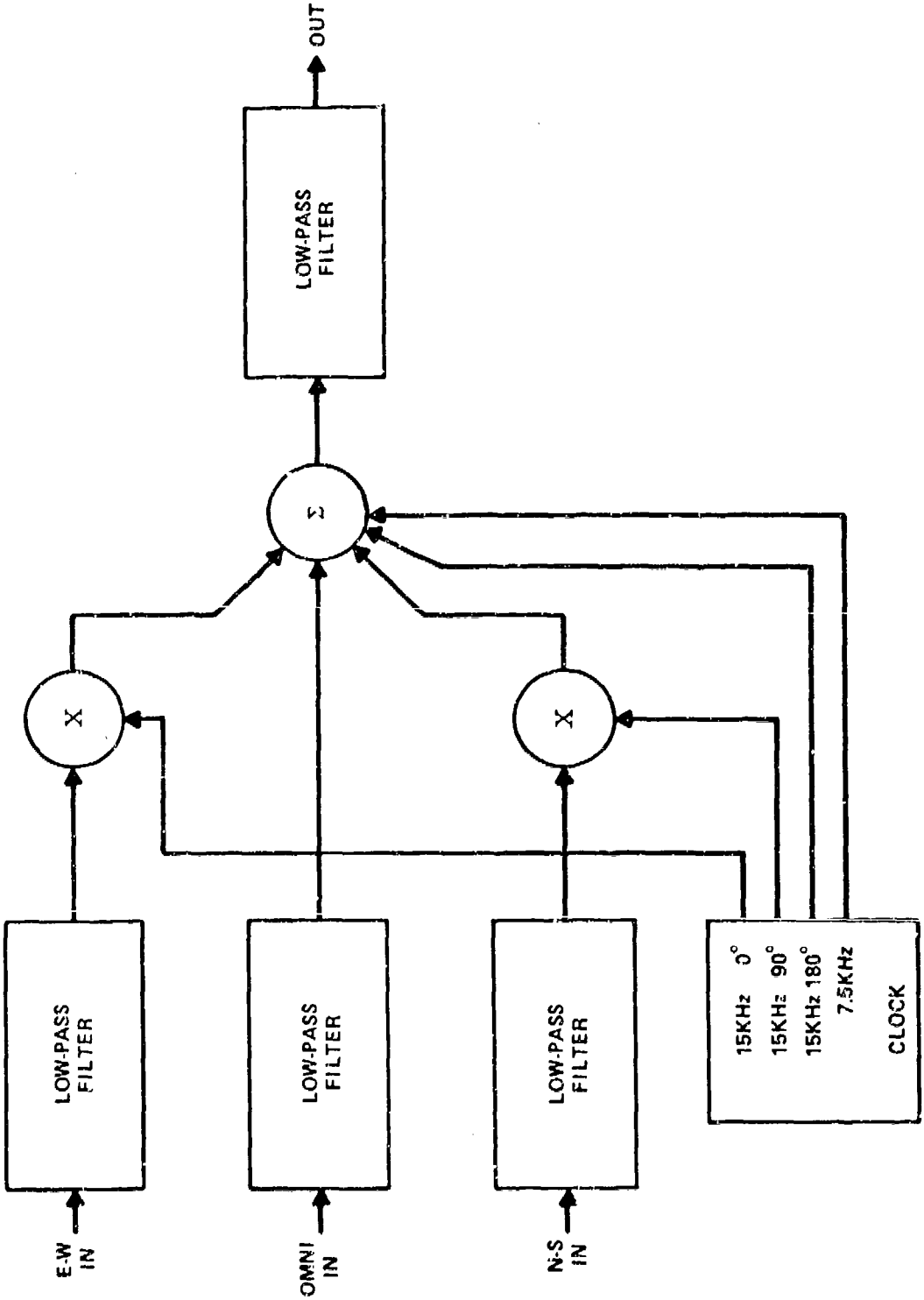


FIGURE 2. MULTIPLEXER BLOCK DIAGRAM

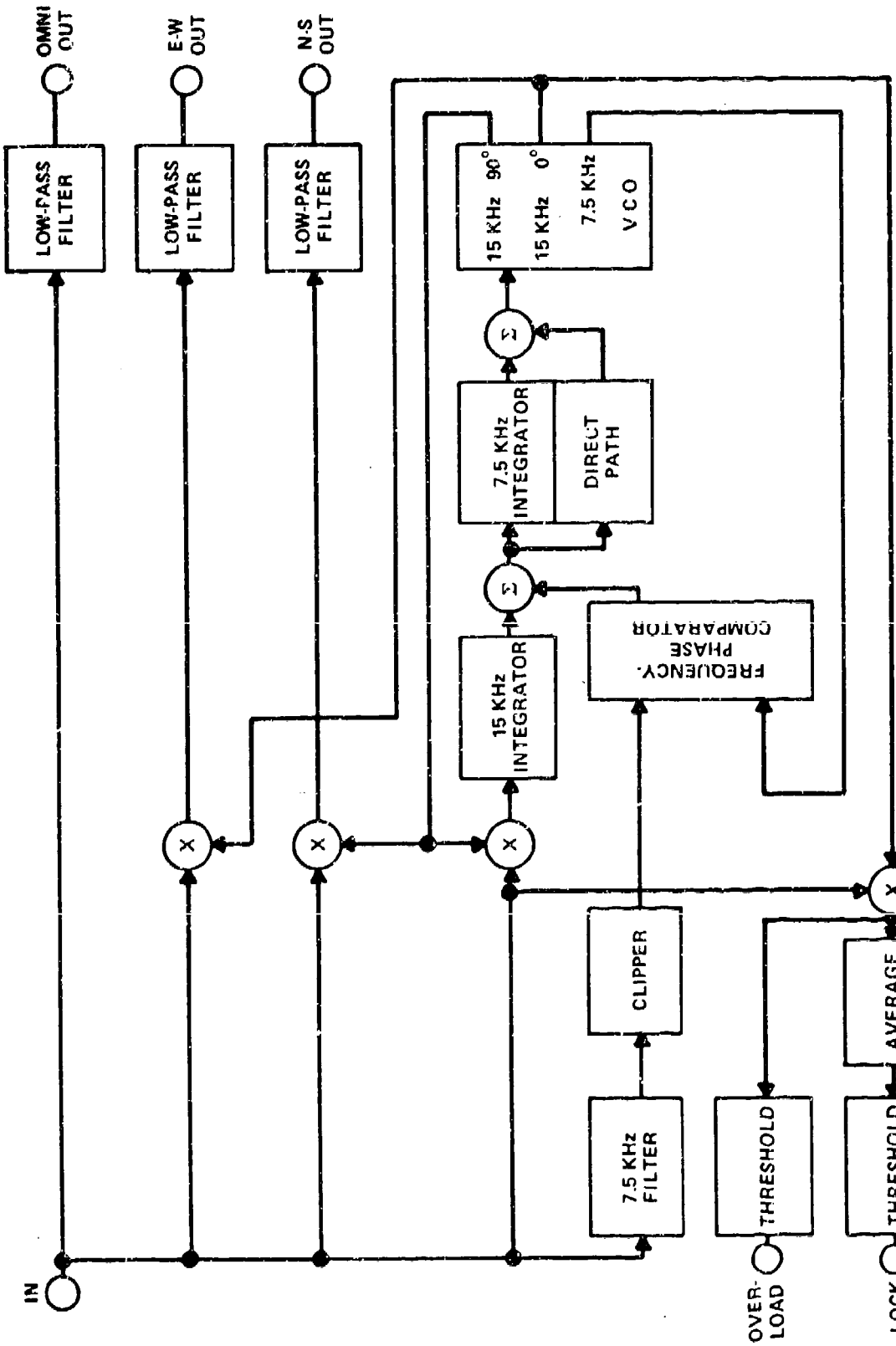
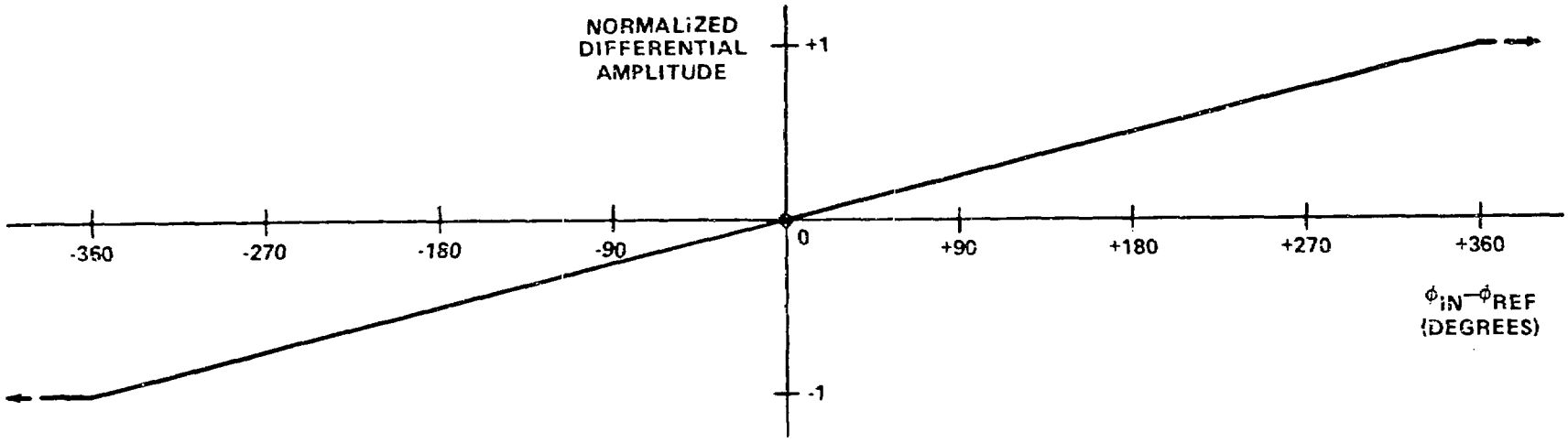
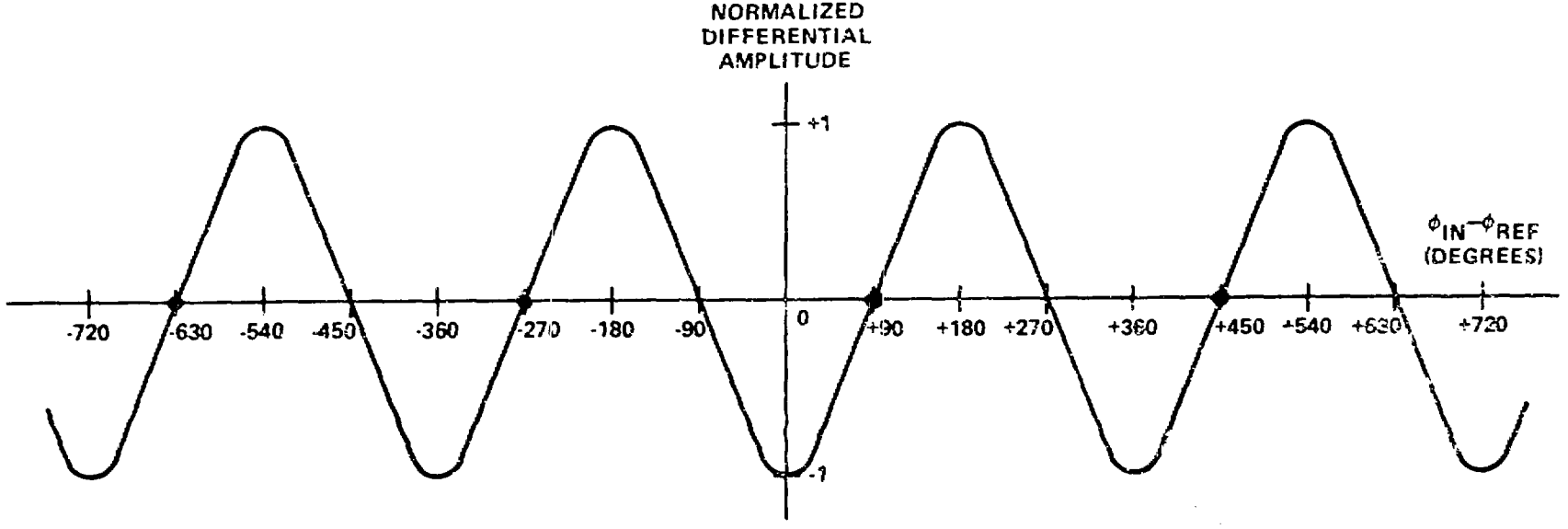


FIGURE 3. DEMULTIPLEXER BLOCK DIAGRAM



a 7.5 KHZ DETECTOR

NOTE: DOTS ARE
EQUILIBRIUM POINTS



b 15 KHZ DETECTOR

FIGURE 4. PHASE DETECTOR OUTPUTS

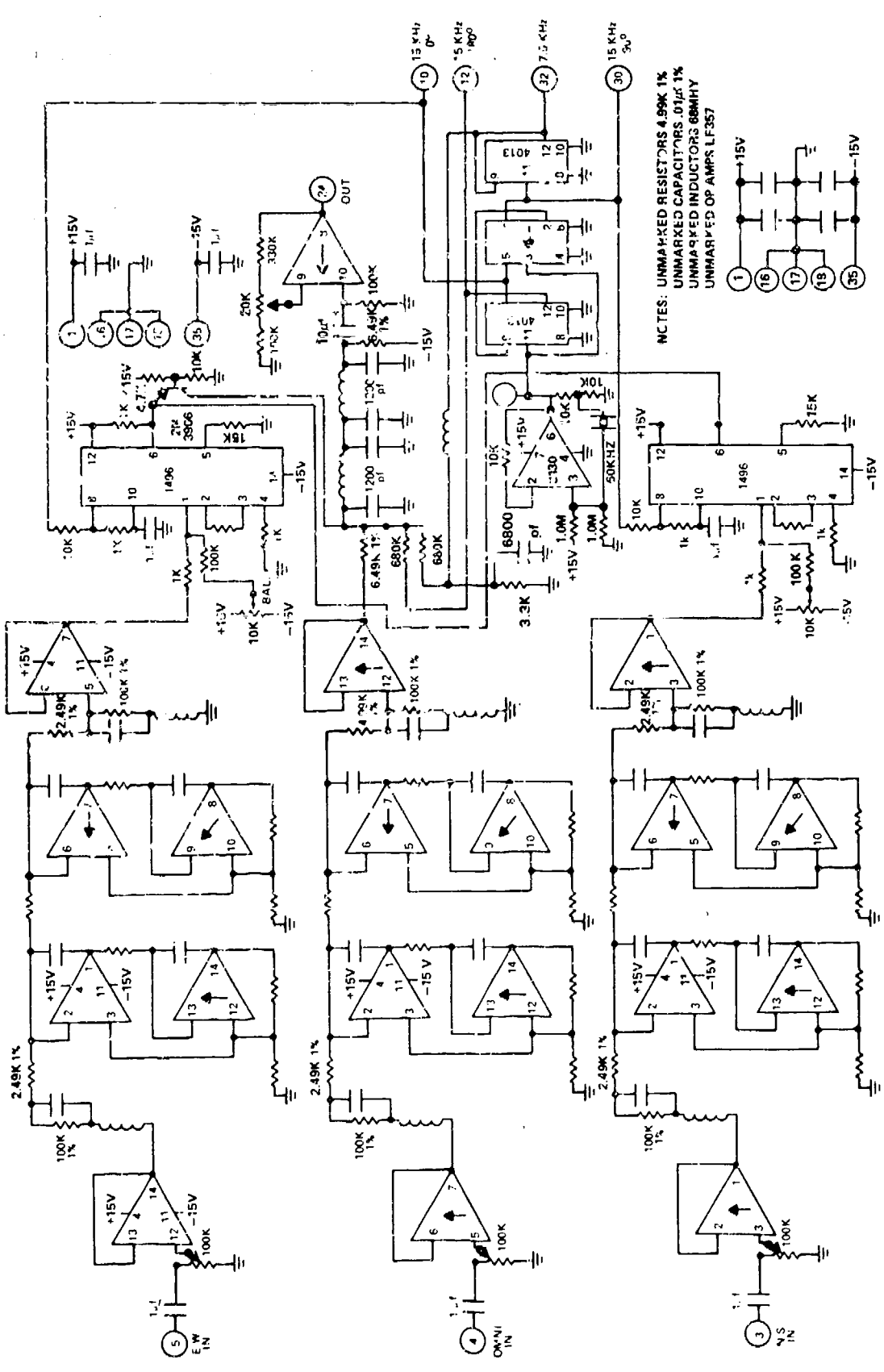


FIGURE 5. MULTIPLEXER CIRCUIT

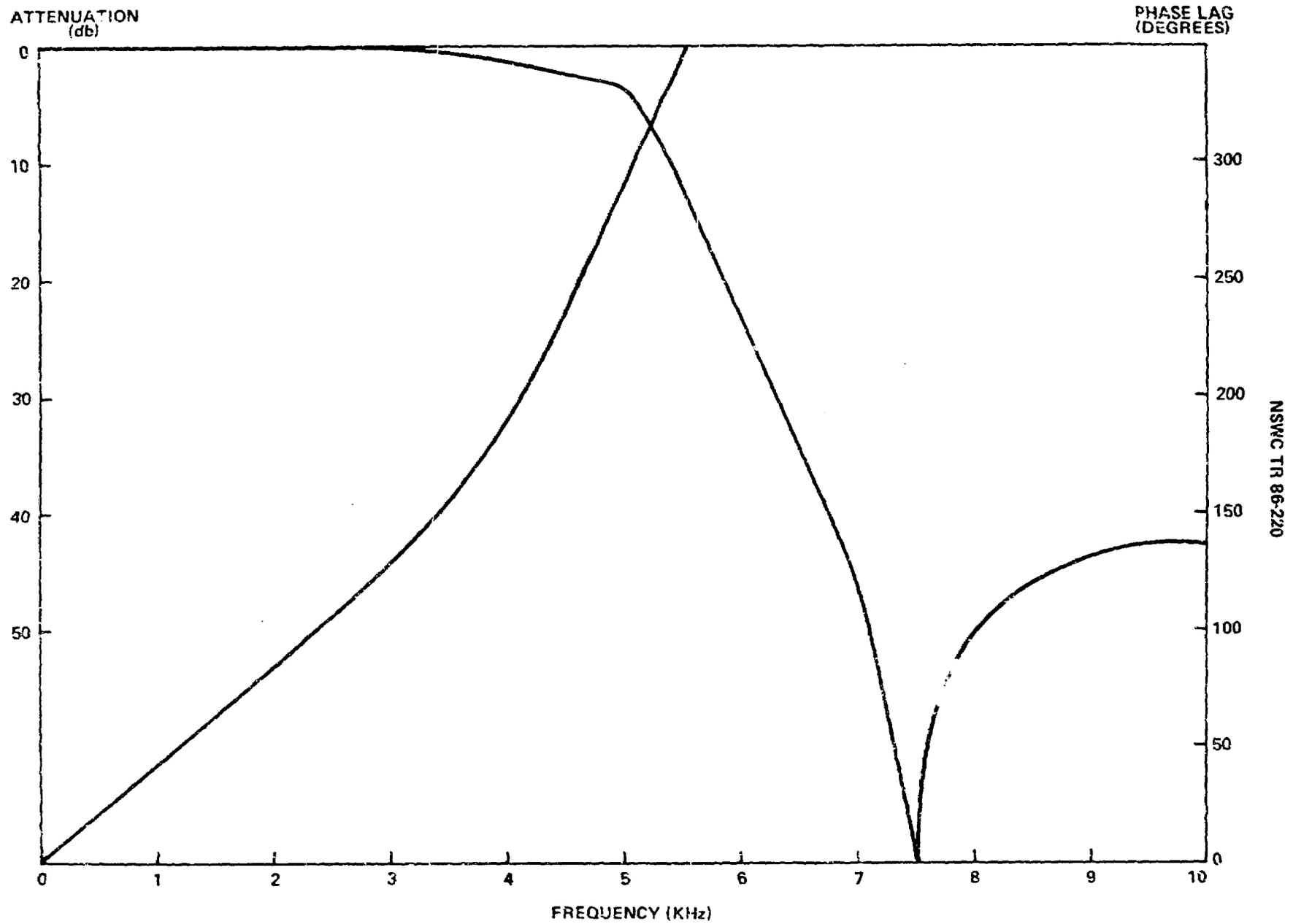


FIGURE 6. MULTIPLEXER INPUT FILTER CHARACTERISTICS

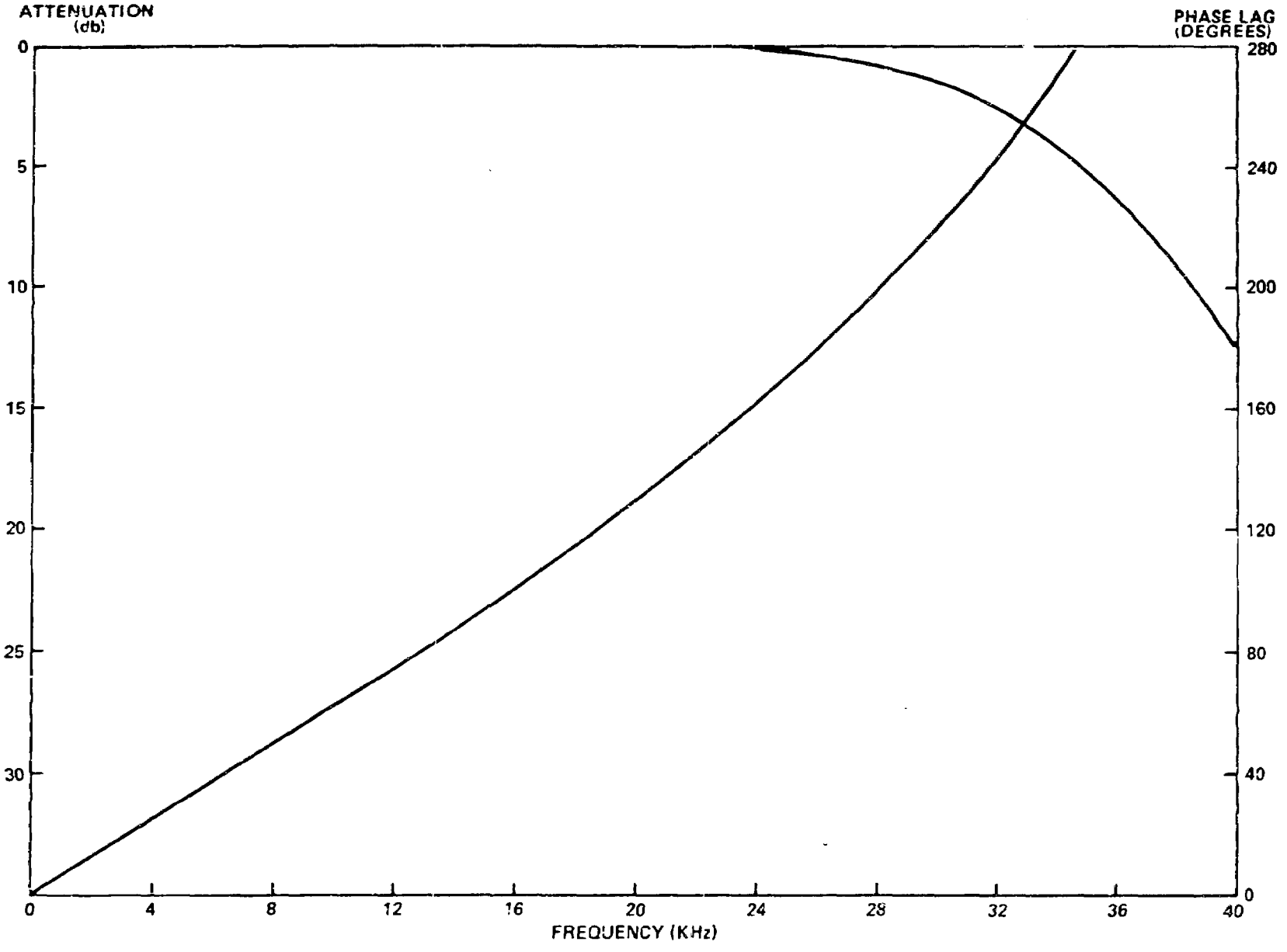


FIGURE 7. MULTIPLEXER OUTPUT FILTER CHARACTERISTICS

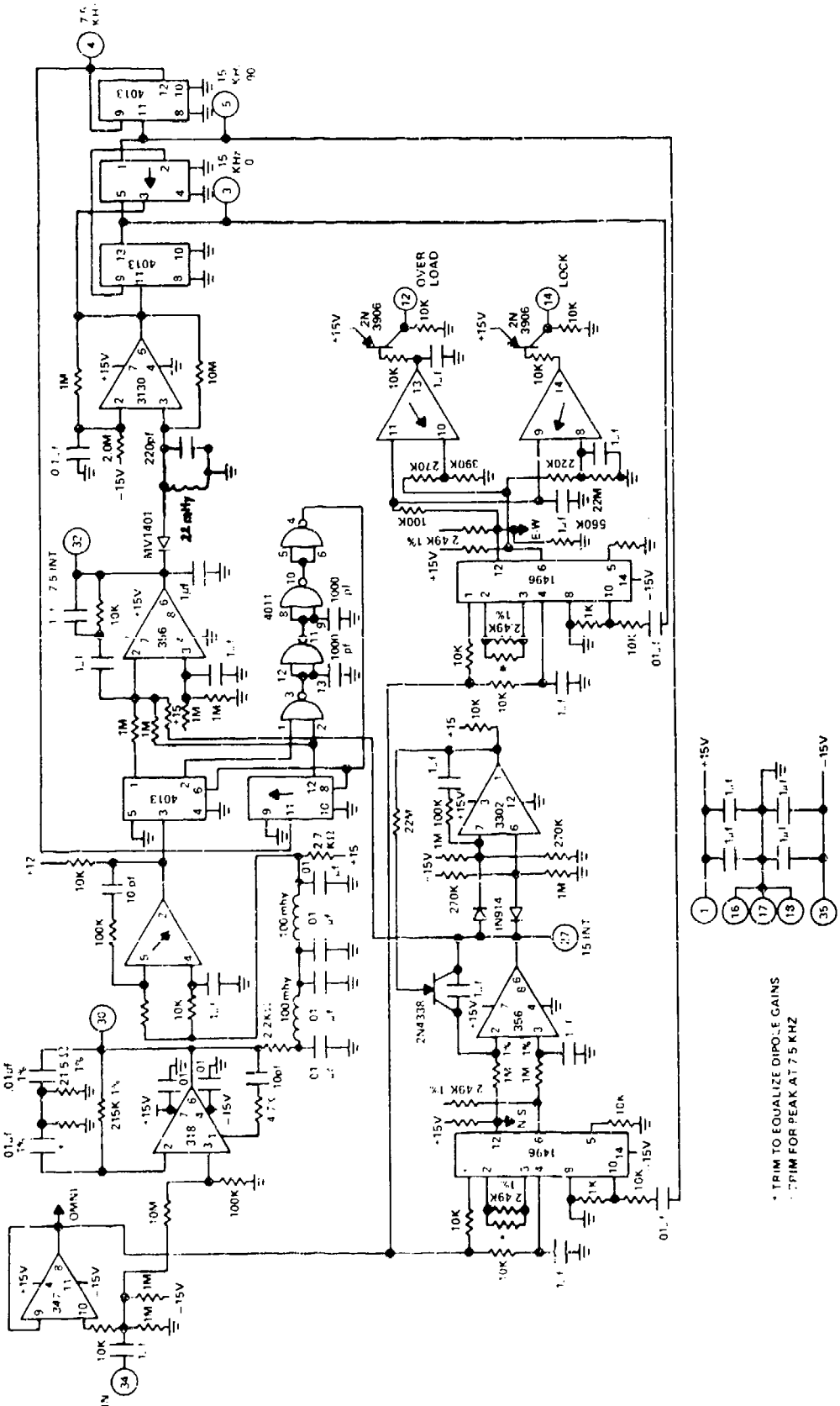
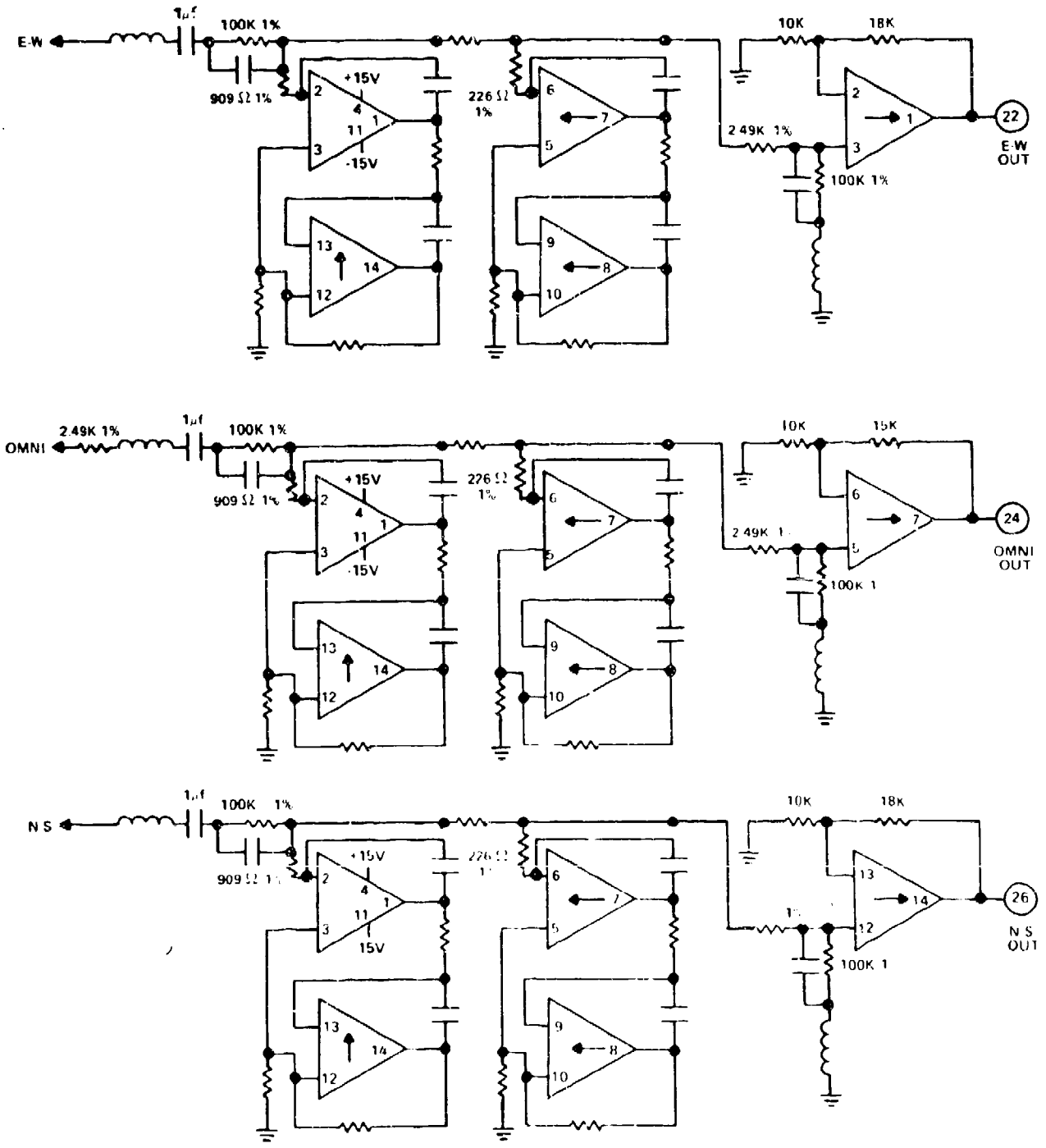
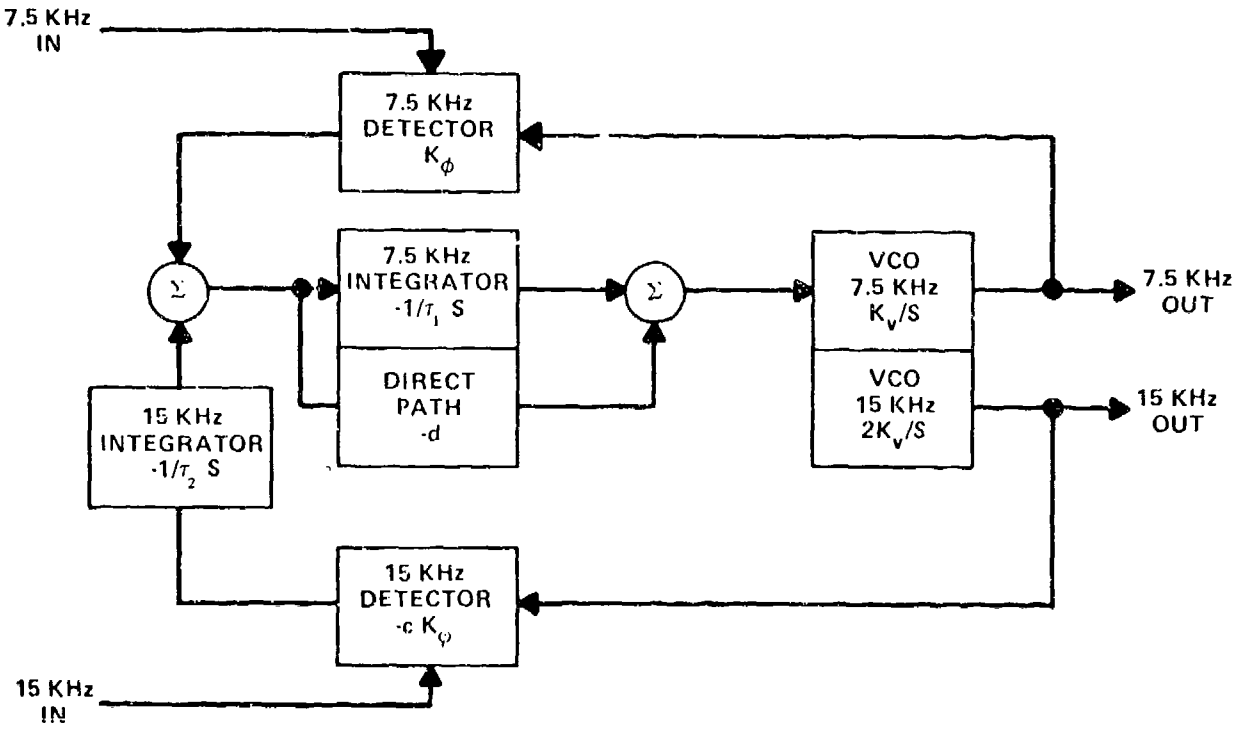


FIGURE 8. DEMULTIPLEXER PHASE-LOCK LOOP CIRCUIT

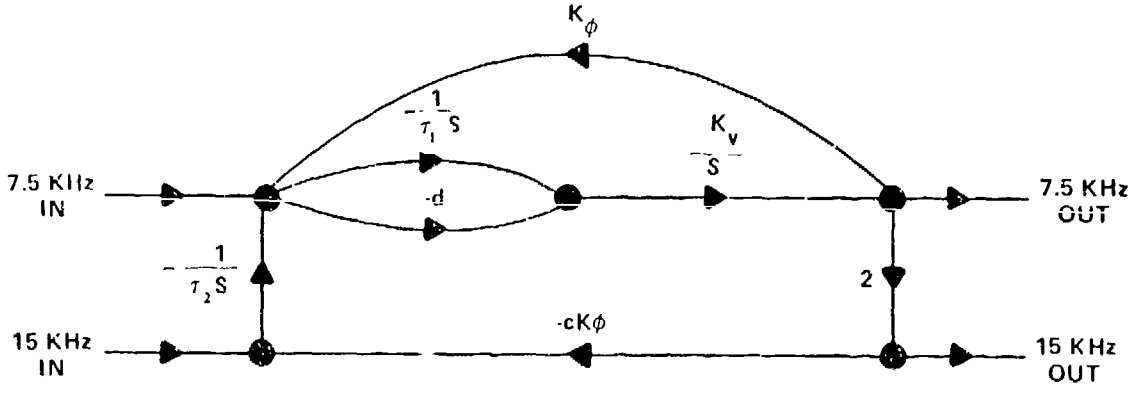


NOTES UNMARKED CAPACITORS .01 1%
UNMARKED RESISTORS 4.99K 1%
ALL INDUCTORS 68 MHY
ALL OP AMPS LF 347

FIGURE 9. DEMULTIPLEXER OUTPUT FILTER CIRCUITS

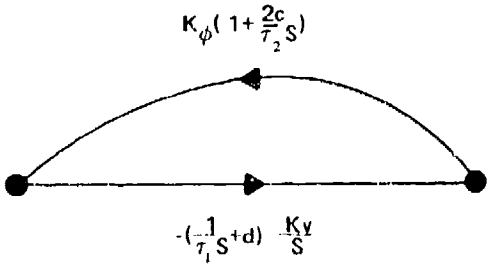


a. BLOCK DIAGRAM

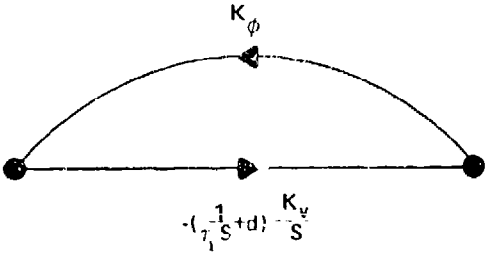


b. FLOW GRAPH

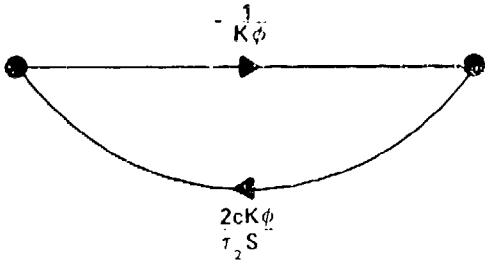
FIGURE 10. LOOP ANALYSIS



a DOUBLE LOOP

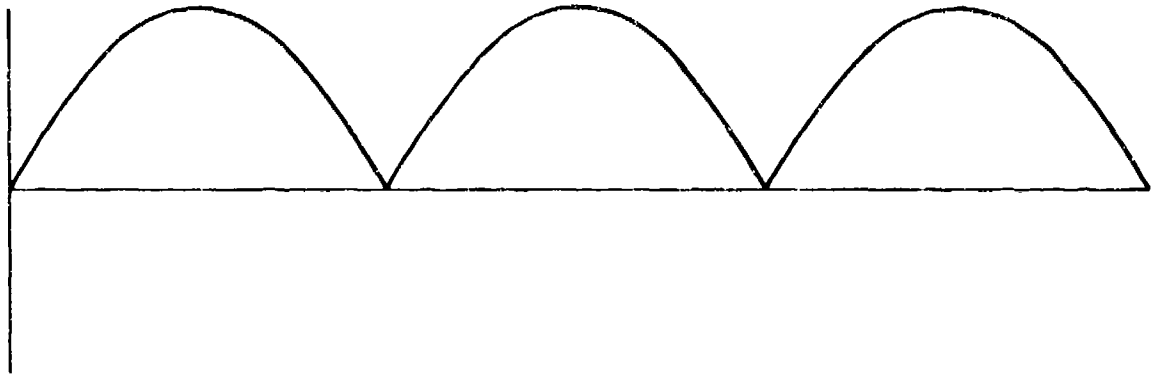


b 7.5 KHz LOOP

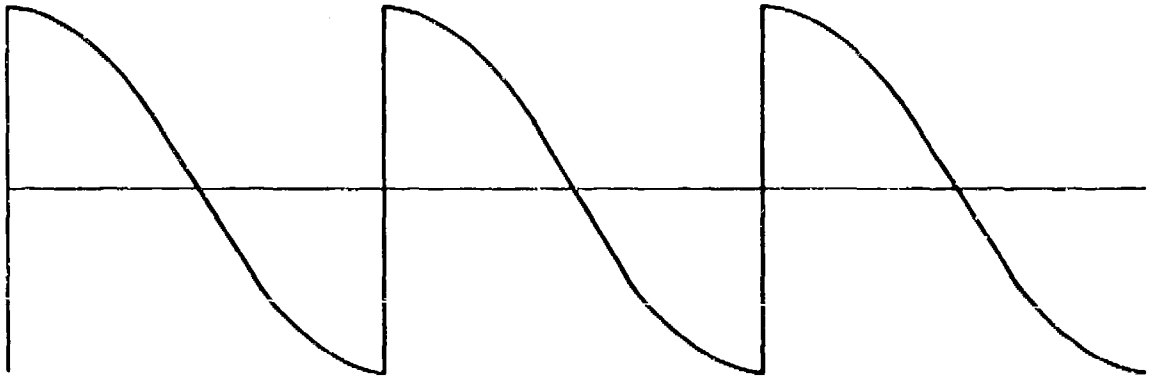


c 15 KHz LOOP

FIGURE 11. SIMPLIFIED FLOW GRAPHS



a. ZERO PHASE DIFFERENCE



b. $\pi/2$ RAD PHASE DIFFERENCE

FIGURE 12. BALANCED MODULATOR WAVEFORMS

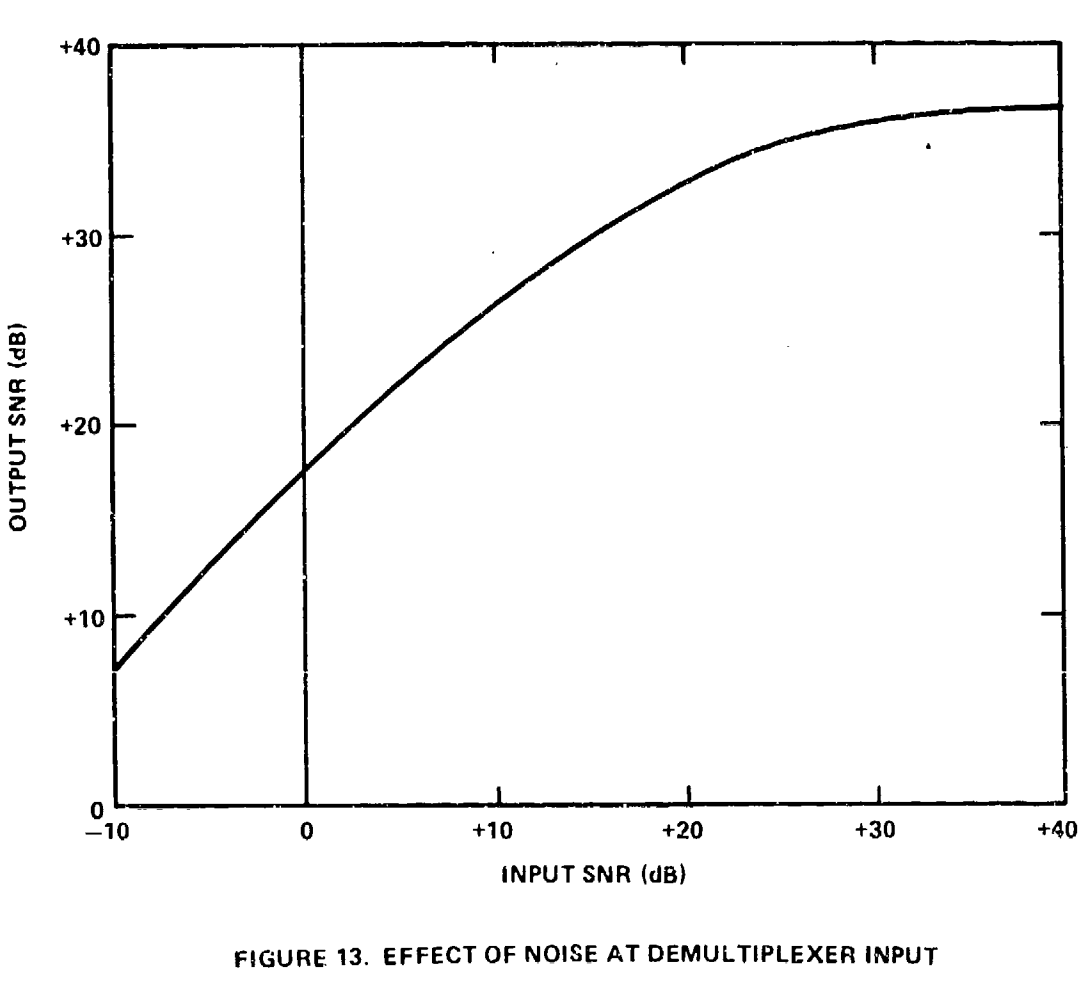


FIGURE 13. EFFECT OF NOISE AT DEMULTIPLEXER INPUT

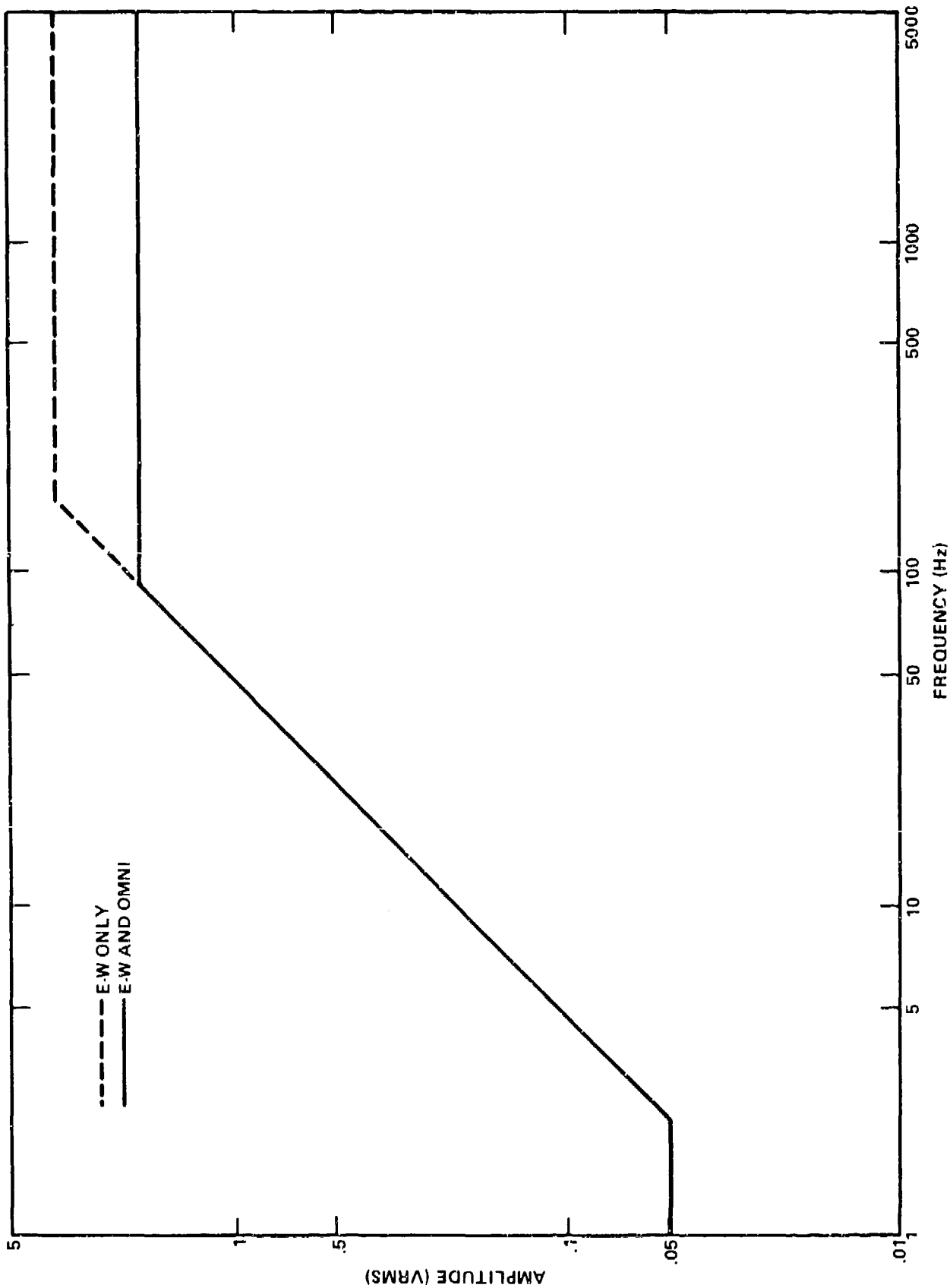


FIGURE 14. ALLOWABLE INPUT AMPLITUDE

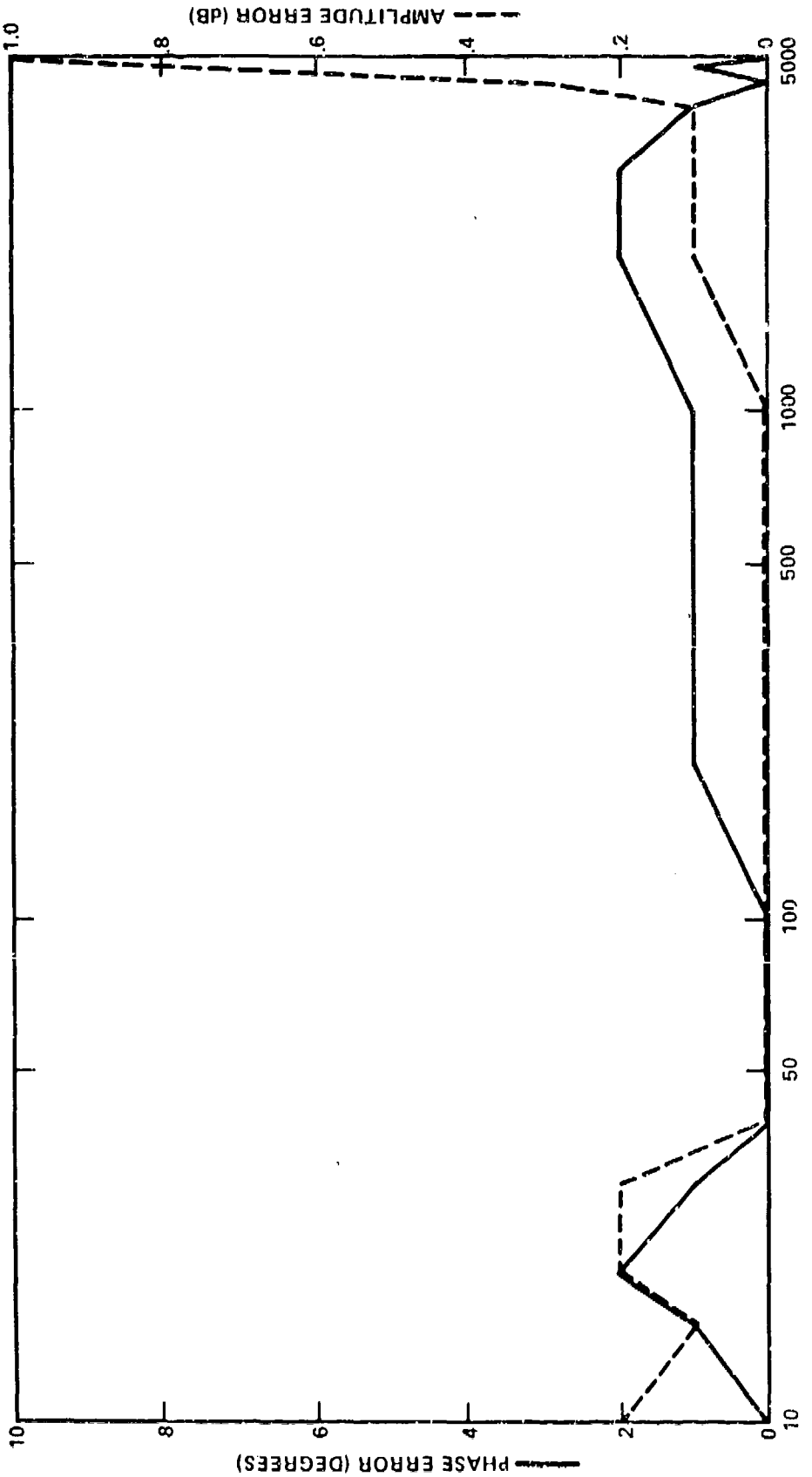


FIGURE 15. N-S TO E-W ERROR

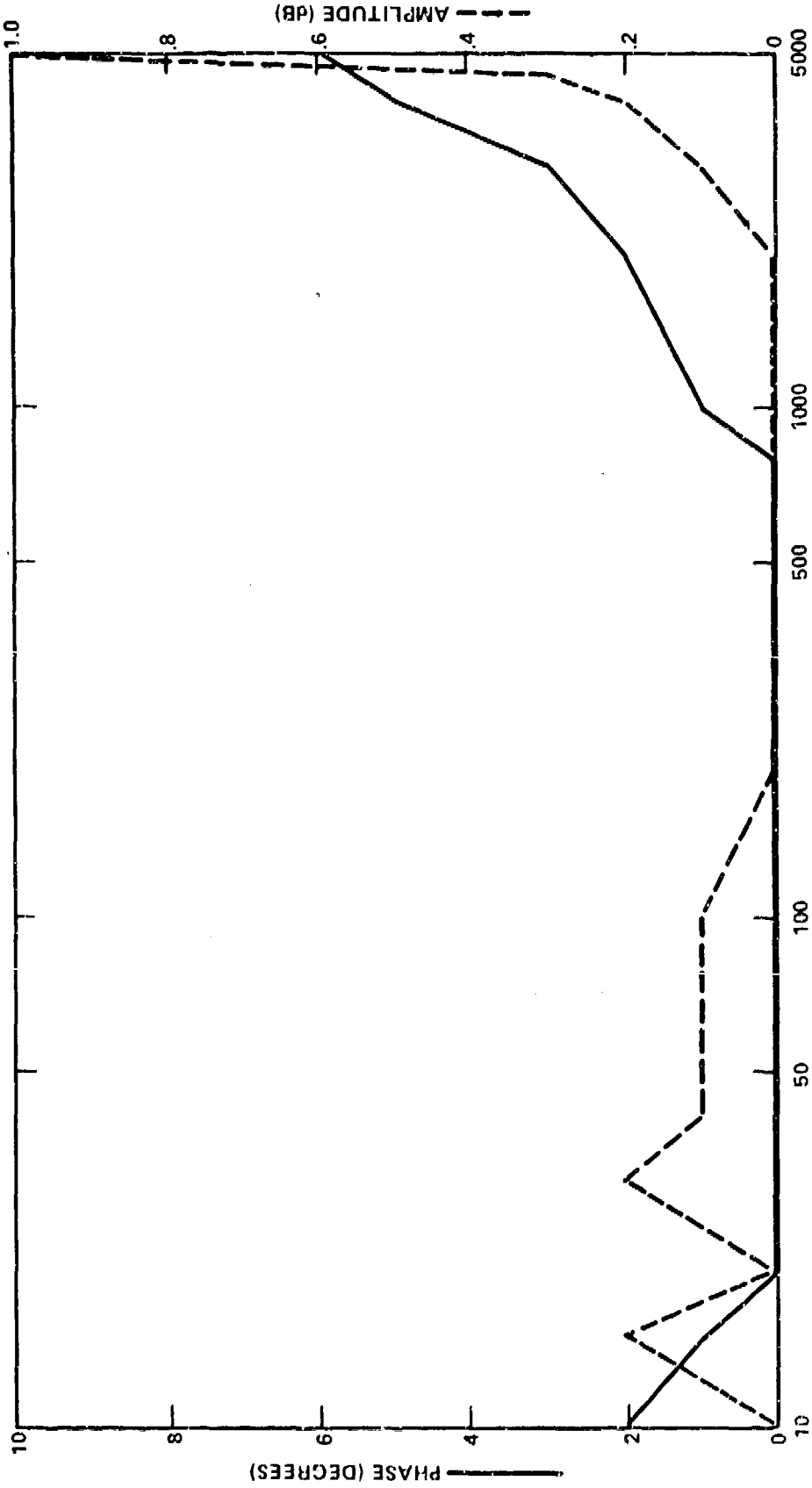


FIGURE 16. N-S TO OMNI ERROR

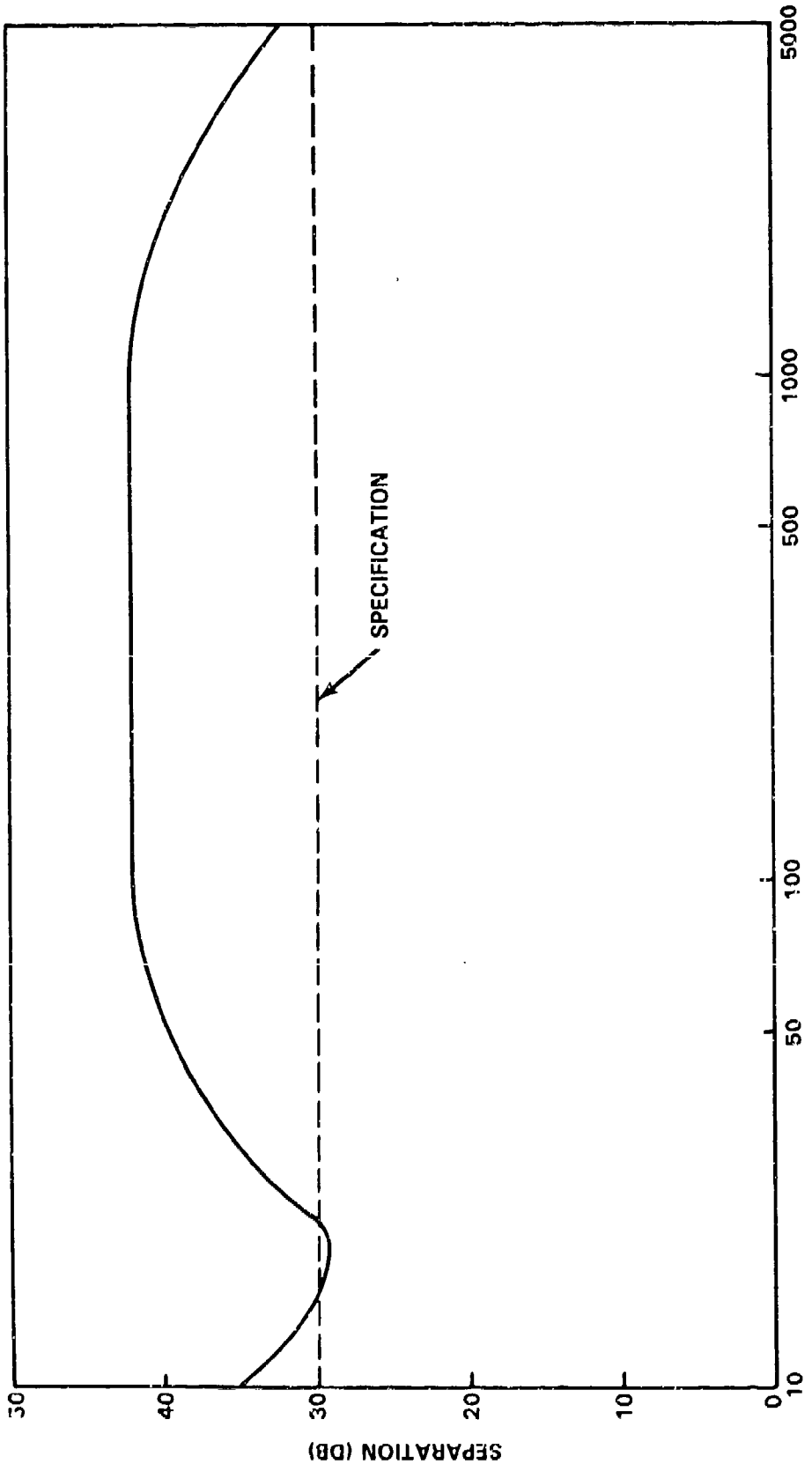


FIGURE 17. DIPOLE SEPARATION VS. FREQUENCY

APPENDIX A
MULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±15V ± 15mV. If supplies cannot be adjusted, card should be adjusted with the same supply it will be operated with.

2. Check oscillator output (pin 20). It should be a squarish waveform, 0 to +15V, 60.000 KHz ± 60 Hz.

3. Set the three input pots all the way up. Observe the output (pin 24) with no signals in. Ground pins 12 and 32. Adjust the two modulator pots (next to the two 1496s) alternately for minimum output signal using a true-RMS AC voltmeter.

4. Ground pin 32 only. Output should be 15 KHz ± 15 Hz, fairly sinusoidal. Adjust output pot (next to 4605) for 100 mVRMS (-20 dB), true-RMS.

5. Ground pin 12 only. Output should be 7.5 KHz ± 7.5 Hz, irregular waveform. Amplitude should be 115 mVRMS ± 15 mVRMS, true-RMS. There is no adjustment.

6. Ground pins 12 and 32. Place a 1 KHz, 1 VRMS sine on N-S in (pin 3). Adjust corresponding input pot for 0.8 VRMS at output (true-RMS). Repeat for E-W in (pin 5). Repeat for OMNI (pin 4).

7. Check frequency response. For each of the three channels, increase input frequency until output level drops 3 dB from that at 1 KHz. Frequency should be 5 KHz ± 0.5 KHz.

8. If a certified demultiplexer is available, check the multiplexer with it. (See Appendix B, step 5a). This is optional.

APPENDIX B
DEMULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±15V ± 15 mV. If supplies cannot be adjusted, card should be adjusted with the same supply it will be operated with.

2. Place a 100mV sine wave on the input (pin 34), about 7.5KHz. Find the frequency f that gives maximum output from the 7.5KHz filter (318, pin 6). Calculate

$$R_{TRIM} = 21.5\Omega \Big/ \left[(7.5\ \text{KHz}/f)^2 - 1\right]$$

and place across the 21.5Ω resistor. Recheck filter to see that it peaks at 7.5KHz ± 7 5Hz.

3. Place a 1 KHz 1 VRMS sine wave on the input. Adjust for 0VDC between the outputs of each 1496 (pins 6 and 12) by the pot next to each. OMNI output (pin 24) should be a 1 KHz 1.45 VRMS ± 0.15 VRMS sine wave. Lock light should not light.

4. Place at the input a composite waveform consisting of 16 KHz 0.5 VRMS sine wave plus a 7.5 KHz 0.5 VRMS rectangular wave of 25% duty cycle. Lock light should light. Overload light should not. N-S (pin 26) and E-W (pin 22) outputs should be sine waves, 1 KHz, 400 mVRMS ± 50 mVRMS, slightly unequal. Calculate

$$R_{TRIM} = 2.49K/(V_{HI}/V_{LO} - 1)$$

where V_{HI} and V_{LO} are the higher and lower readings, respectively. Add R_{TRIM} to the demodulator (1496 pins 2 and 3) having the lower output. (N-S is closer to the card connector). Recheck the two outputs. They should be equal within 0.1 dB. Increase input composite waveform to 5 VRMS by increasing either generator output 20 dB. Overload light should come on.

5. (a) Connect a certified multiplexer to the demultiplexer. Place a 1 KHz 1 VRMS sine wave on the N-S input. Lock light should be lit. Overload light should not. Readjust pot nearest card connector (demultiplexer) to minimize the 1 KHz signal at the E-W output. Check to see that the 1 KHz 1 VRMS input signal appears at the N-S output. Move input signal to E-W input and check to see that it appears at E-W output. Move to OMNI input and check to see that it appears at OMNI output. Output level should be the same within 0.3 dB for all three cases. Check frequency response for all three channels. It should be down 6 dB at 5 KHz ± 0.5 KHz. Check feedthrough and noise at the outputs with no signals in. It should be below -50 dB re 1 VRMS for each, true RMS.

   (b) If a certified multiplexer is not available, proceed as follows: Check the frequency response of the OMNI by inserting the signal of step (3) but increasing the frequency until the OMNI output amplitude drops 3 dB.

Frequency should be 5 KHz ± 0.5 KHz. Check the frequency response of each dipole by inserting the composite signal of step (4) but increasing the sine wave frequency until the output amplitude drops 3 dB. Output frequency should be 5 KHz ± 0.5 KHz. Check feedthrough and noise by observing the three outputs with no signal into the demultiplexer. It should be below -50 dB re 1 VRMS for each, true RMS. There is no independent method for balancing the loop precisely, so some additional phase error will result if the demultiplexer has not been tested with a multiplexer.

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